L Number	Hits	Search Text	DB	Time stamp
3	10859	(gate near3 (floating control)) with (oxide dieletric tunnel$)	USPAT; US-PGPUB	2004/08/10 13:51
4	58	((gate near3 (floating control)) with (oxide dieletric tunnel$)) with plug	USPAT; US-PGPUB	2004/08/10 13:52

EAST - [2268.wsp:1]

File View Edit Tools Window Help

Drafts
Pending
Active
L3: (10859)

Search | List | Browse | Queue | Clear

DBs | USPAT; US-PGPUB | Plurals

Default operator: OR | Highlight all hit terms initially

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 20040132251 A1	20040708	66	Non-volatile memory and method for manufacturing non-volatile memory	438/267	
2	☐	☐	US 20040121573 A1	20040624	10	Method for forming enhanced areal density split gate field effect transistor	438/594	438/266
3	☐	☐	US 20040087084 A1	20040506	16	Self-aligned structure with unique erasing gate in split gate flash	438/257	
4	☐	☐	US 20040077144 A1	20040422	16	Method to form self-aligned split gate flash with L-shaped wordline spacers	438/257	
5	☐	☐	US 20040076050 A1	20040422	19	Flash memory cell with high programming efficiency by coupling f	365/200	
6	☐	☐	US 20040056316 A1	20040325	15	Method and apparatus for a flash memory device comprising a source l	257/390	257/324; 257/391
7	☐	☐	US 20040053455 A1	20040318	12	System and method for forming a semiconductor with an analog capacit	438/197	
8	☐	☐	US 20040029319 A1	20040212	14	METHOD TO REMOVE AN OXIDE SEAM ALONG GATE STA	438/142	257/E21.682; 257/E27.103
9	☐	☐	US 20040014286 A1	20040122	13	Method of forming a select line in a NAND type flash memory device	438/264	
10	☐	☐	US 20030223299 A1	20031204	10	Method of forming twin-spacer gate FLASH device and the structure of th	365/203	
11	☐	☐	US 20030092237 A1	20030515	9	Process for manufacturing non-volatile memory cells integrated o	438/257	257/E21.682; 438/259
12	☐	☐	US 20030075756 A1	20030424	9	Nonvolatile semiconductor memory device and its manufacturing method	257/315	257/316; 257/317;

Start 4:01 PM

EAST - [2268.wsp:1]

File View Edit Tools Window Help

Drafts
Pending
Active
L3: (10859)

Search | List | Browse | Queue | Clear

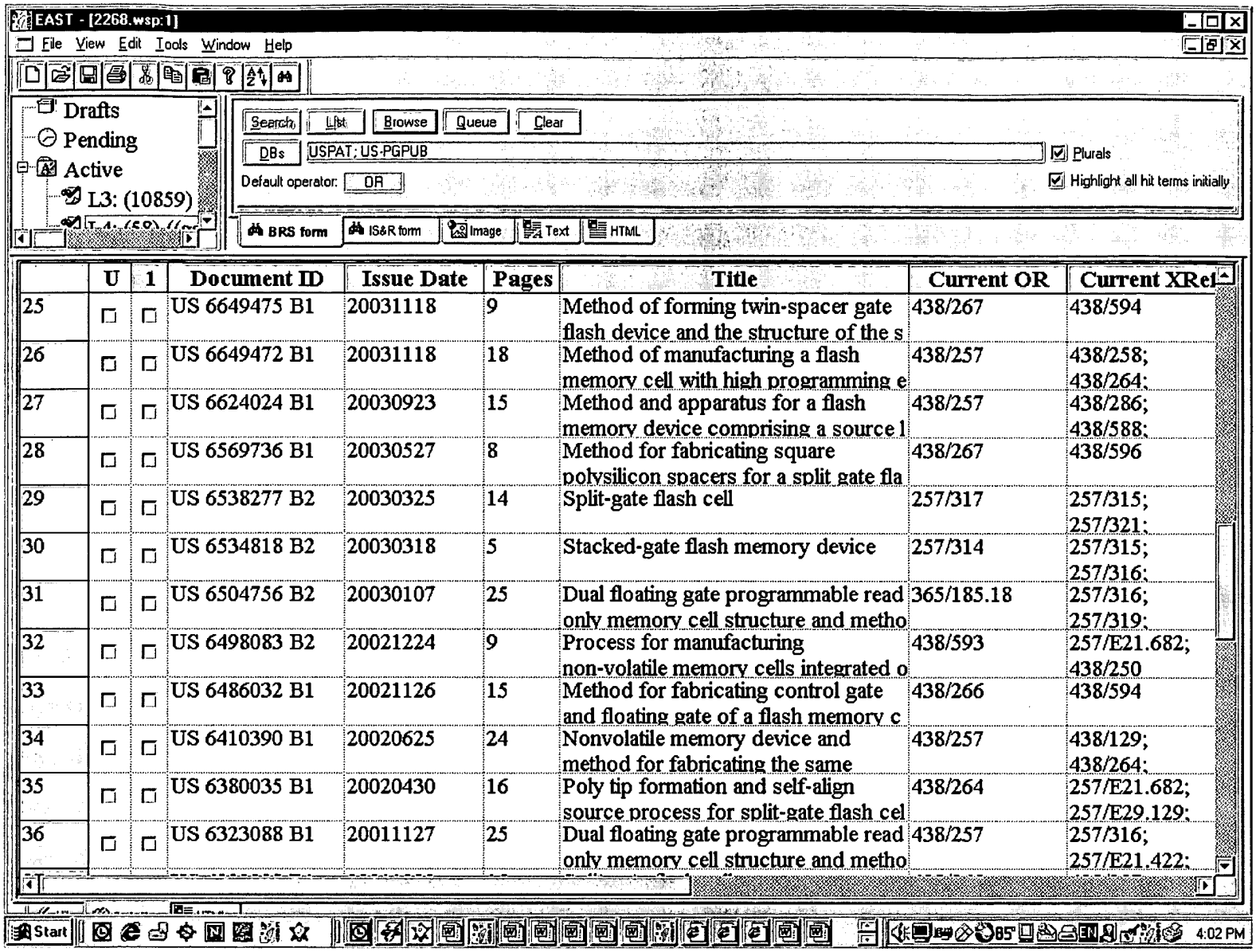
DBs | USPAT; US-PGPUB | Plurals

Default operator: OR | Highlight all hit terms initially

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
13	☐	☐	US 20030042520 A1	20030306	29	Semiconductor integrated circuit device and a method of manufacturin	257/296	257/E21.688; 257/E27.081
14	☐	☐	US 20030030096 A1	20030213	6	STACKED-GATE FLASH MEMORY DEVICE	257/314	257/296; 257/302;
15	☐	☐	US 20030003662 A1	20030102	19	Nonvolatile storage device and method for manufacturing nonvolatile	438/264	257/324; 257/E29.129;
16	☐	☐	US 20020132410 A1	20020919	26	Nonvolatile memory device and method for fabricating the same	438/201	438/211; 438/257
17	☐	☐	US 20020027241 A1	20020307	16	Novel split-gate flash cell	257/314	257/324
18	☐	☐	US 20010046164 A1	20011129	28	Dual floating gate programmable read only memory cell structure and metho	365/200	257/E21.422; 257/E29.308
19	☐	☐	US 20010016379 A1	20010823	9	Process for manufacturing non-volatile memory cells integrated o	438/211	257/E21.682
20	☐	☐	US 6762452 B2	20040713	9	Non-volatile memory cells integrated on a semiconductor substrate	257/316	257/314; 257/315;
21	☐	☐	US 6756271 B1	20040629	22	Simplified twin monos fabrication method with three extra masks to stan	438/258	438/954
22	☐	☐	US 6720779 B1	20040413	21	Defect type identification using hyper-extracting-field	324/751	
23	☐	☐	US 6713350 B2	20040330	13	Method to remove an oxide seam along gate stack edge, when nitride sp	438/261	257/E21.682; 257/E27.103;
24	☐	☐	US 6677638 B2	20040113	23	Nonvolatile memory device and method for fabricating the same	257/314	257/315; 257/324;

Start 4:01 PM



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
25	☐	☐	US 6649475 B1	20031118	9	Method of forming twin-spacer gate flash device and the structure of the s	438/267	438/594
26	☐	☐	US 6649472 B1	20031118	18	Method of manufacturing a flash memory cell with high programming e	438/257	438/258; 438/264;
27	☐	☐	US 6624024 B1	20030923	15	Method and apparatus for a flash memory device comprising a source l	438/257	438/286; 438/588;
28	☐	☐	US 6569736 B1	20030527	8	Method for fabricating square polysilicon spacers for a split gate fla	438/267	438/596
29	☐	☐	US 6538277 B2	20030325	14	Split-gate flash cell	257/317	257/315; 257/321;
30	☐	☐	US 6534818 B2	20030318	5	Stacked-gate flash memory device	257/314	257/315; 257/316;
31	☐	☐	US 6504756 B2	20030107	25	Dual floating gate programmable read only memory cell structure and metho	365/185.18	257/316; 257/319;
32	☐	☐	US 6498083 B2	20021224	9	Process for manufacturing non-volatile memory cells integrated o	438/593	257/E21.682; 438/250
33	☐	☐	US 6486032 B1	20021126	15	Method for fabricating control gate and floating gate of a flash memory c	438/266	438/594
34	☐	☐	US 6410390 B1	20020625	24	Nonvolatile memory device and method for fabricating the same	438/257	438/129; 438/264;
35	☐	☐	US 6380035 B1	20020430	16	Poly tip formation and self-align source process for split-gate flash cel	438/264	257/E21.682; 257/E29.129;
36	☐	☐	US 6323088 B1	20011127	25	Dual floating gate programmable read only memory cell structure and metho	438/257	257/316; 257/E21.422;

EAST - [2268.wsp:1]

File View Edit Tools Window Help

Drafts
Pending
Active
L3: (10859)

Search | List | Browse | Queue | Clear

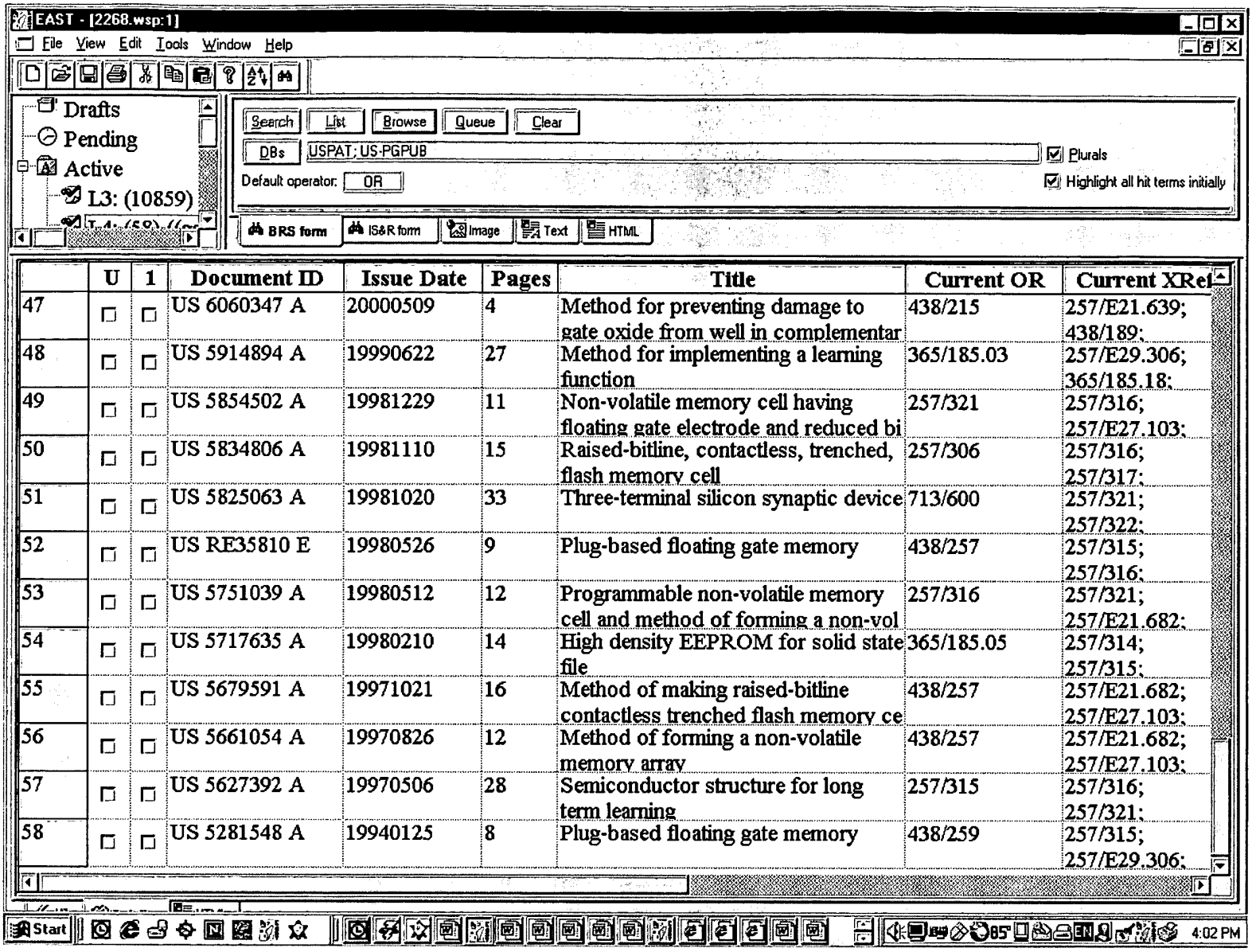
DBs | USPAT; US-PGPUB | Plurals

Default operator: OR | Highlight all hit terms initially

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
37	☐	☐	US 6309928 B1	20011030	15	Split-gate flash cell	438/265	438/257; 438/259;
38	☐	☐	US 6294429 B1	20010925	9	Method of forming a point on a floating gate for electron injection	438/260	257/317; 257/E21.193;
39	☐	☐	US 6285577 B1	20010904	8	Non-volatile memory using ferroelectric capacitor	365/145	257/E27.104; 365/65
40	☐	☐	US 6284597 B1	20010904	7	Method of fabricating flash memory	438/257	257/E21.682; 438/261;
41	☐	☐	US 6259131 B1	20010710	15	Poly tip and self aligned source for split-gate flash cell	257/315	257/321; 257/322;
42	☐	☐	US 6255165 B1	20010703	11	Nitride plug to reduce gate edge lifting	438/257	257/E21.193; 257/E21.209;
43	☐	☐	US 6178113 B1	20010123	27	Dual floating gate programmable read only memory cell structure and metho	365/185.03	257/316; 257/319;
44	☐	☐	US 6137133 A	20001024	12	Programmable non-volatile memory cell and method of forming a non-vol	257/316	257/321; 257/E21.682;
45	☐	☐	US 6117733 A	20000912	18	Poly tip formation and self-align source process for split-gate flash cel	438/265	257/288; 257/314;
46	☐	☐	US 6117728 A	20000912	11	Programmable non-volatile memory cell and method of forming a non-vol	438/257	257/E21.682; 257/E27.103;
47	☐	☐	US 6060347 A	20000509	4	Method for preventing damage to gate oxide from well in complementar	438/215	257/E21.639; 438/189;
48	☐	☐	US 5914894 A	19990622	27	Method for implementing a learning function	365/185.03	257/E29.306; 365/185.18;

Start 4:02 PM



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
47	☐	☐	US 6060347 A	20000509	4	Method for preventing damage to gate oxide from well in complementar	438/215	257/E21.639; 438/189;
48	☐	☐	US 5914894 A	19990622	27	Method for implementing a learning function	365/185.03	257/E29.306; 365/185.18;
49	☐	☐	US 5854502 A	19981229	11	Non-volatile memory cell having floating gate electrode and reduced bi	257/321	257/316; 257/E27.103;
50	☐	☐	US 5834806 A	19981110	15	Raised-bitline, contactless, trenched, flash memory cell	257/306	257/316; 257/317;
51	☐	☐	US 5825063 A	19981020	33	Three-terminal silicon synaptic device	713/600	257/321; 257/322;
52	☐	☐	US RE35810 E	19980526	9	Plug-based floating gate memory	438/257	257/315; 257/316;
53	☐	☐	US 5751039 A	19980512	12	Programmable non-volatile memory cell and method of forming a non-vol	257/316	257/321; 257/E21.682;
54	☐	☐	US 5717635 A	19980210	14	High density EEPROM for solid state file	365/185.05	257/314; 257/315;
55	☐	☐	US 5679591 A	19971021	16	Method of making raised-bitline contactless trenched flash memory ce	438/257	257/E21.682; 257/E27.103;
56	☐	☐	US 5661054 A	19970826	12	Method of forming a non-volatile memory array	438/257	257/E21.682; 257/E27.103;
57	☐	☐	US 5627392 A	19970506	28	Semiconductor structure for long term learning	257/315	257/316; 257/321;
58	☐	☐	US 5281548 A	19940125	8	Plug-based floating gate memory	438/259	257/315; 257/E29.306;